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DERWENT-WEEK: 200016

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TITLE: Special purpose software data model optimized for a
static timing analysis and related problems such as the
timing graph

PATENT-ASSIGNEE: ANONYMOUS[ANON]

PRIORITY-DATA: 1999RD-0429080 (December 20, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
RD 429080 A	January 10, 2000	N/A	002	H03K 000/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
RD 429080A	N/A	1999RD-0429080	December 20, 1999

INT-CL (IPC): H03K000/00

ABSTRACTED-PUB-NO: RD 429080A

BASIC-ABSTRACT:

NOVELTY - A timing graph is a software description of sequential digital logic for static timing analysis based on three types of primitives, while timing nodes are points on which timing is interesting. Timing analysis is a two-step process, first the design is transferred to a timing graph and static timing analysis is applied to it. A single timing graph data model separates modeling from analysis enabling modularization of the timing analysis system and the analysis engine can be applied to all design abstraction levels including gate and device levels and hierarchy chip or layout.

USE - Static timing analysis using special purpose software models.

ADVANTAGE - Clean analytical algorithm with reduced cost and time.

DESCRIPTION OF DRAWING(S) - The drawing shows the timing graph for a full chip.

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS: SPECIAL PURPOSE SOFTWARE DATA MODEL STATIC TIME ANALYSE
RELATED
PROBLEM TIME GRAPH

DERWENT-CLASS: T01 U21 U22

EPI-CODES: T01-J15A1; T01-S02; U21-C03D1; U22-D03C;

SECONDARY-ACC-NO:

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